ESPS31-32

Product Specification

2.4 GHz Wi-Fi 6 & Bluetooth 5.4 & 802.15.4 Coexistence Module

Version: 1.0 Date: Sep. 30, 2026

Features

- General
  - Chip: ESP32-S31NRV32/S31NRV16
  - Module Size: 18 mm × 25.5 mm × 3 mm
  - Dual-core RISC-V HP processor, up to 320 MHz
  - 32MByte/16MByte PSRAM
  - 320 KB ROM; LP RISC-V core, up to 40 MHz
  - 512 KB HP SRAM + 32 KB LP SRAM
- Wi-Fi Features
  - 2.4 GHz Wi-Fi 6; IEEE 802.11 b/g/n/ax
  - Operating channel frequencies: 2412–2484 MHz
  - Single-stream (1T1R) wireless connectivity
  - TX/RX A-MPDU and A-MSDU aggregation
  - WPA3 security; features depend on firmware
- Bluetooth Features
  - Bluetooth 5.4: LE and Classic Bluetooth
  - Bluetooth LE PHY: 125 kbps, 500 kbps, 1 Mbps, 2 Mbps
  - LE advertising extensions
  - Multiple advertising sets
  - Wi-Fi / Bluetooth / 802.15.4 coexistence
- IEEE 802.15.4
  - IEEE 802.15.4 radio
  - 2.4 GHz O-QPSK PHY
  - Data rate: 250 kbps
  - Thread 1.4
  - Zigbee 3.0
- Peripheral Interfaces
  - 54 GPIO;
  - I2C;
  - I2S;
  - SD/MMC;
  - CAN FD;
  - SPI;
  - UART; USB;
  - MCPWM;
  - ADC;
  - LED PWM;
- 3.3 V nominal power supply

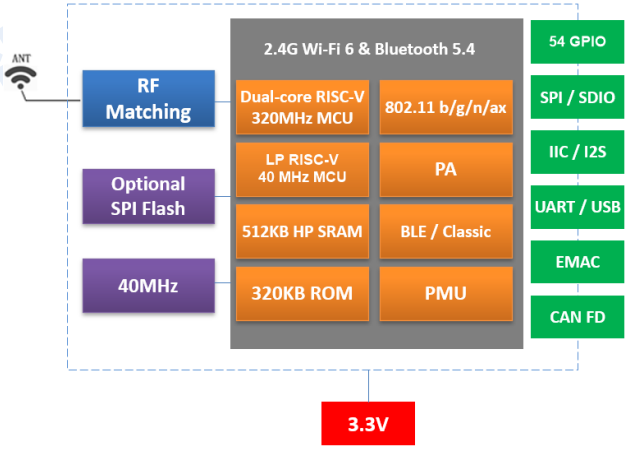
Applications

- Smart home gateways;
- Industrial control and automation;
- Smart lighting and power outlets;
- Connected cameras and displays;
- Sensor networks;
- Audio and multimedia devices;
- Wireless human-machine interfaces;
- IoT protocol bridges;

Module Type

Name	PSRAM	Flash	Antenna
ESPS31-32-N4R16	16 MB	4 MB	PCB
ESPS31-32-N8R16	16 MB	8 MB	PCB
ESPS31-32-N16R16	16 MB	16 MB	PCB
ESPS31-32-N4R32	32 MB	4 MB	PCB
ESPS31-32-N8R32	32 MB	8 MB	PCB
ESPS31-32-N16R32	32 MB	16 MB	PCB

Module Structure



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Update Record

Date	Version	Description
2026-09-30	V1.0	Initial release

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1. Introduction

ESPS31-32 is a compact wireless module based on the ESP32-S31 system-on-chip. It integrates 2.4 GHz Wi-Fi 6, Bluetooth 5.4 and an IEEE 802.15.4 radio, together with a PCB antenna and a 40 MHz crystal. The module measures 18 mm × 25.5 mm × 3 mm and operates from a nominal 3.3 V supply.

The ESP32-S31 includes a dual-core high-performance RISC-V processor operating at up to 320 MHz and a low-power RISC-V core operating at up to 40 MHz. On-chip memory includes 320 KB ROM, 512 KB HP SRAM and 32 KB LP SRAM. ESPS31-32 uses the ESP32-S31 variant with 32 MB/16 MB of in-package PSRAM.

Wireless connectivity includes IEEE 802.11 b/g/n/ax, Bluetooth LE, Classic Bluetooth and IEEE 802.15.4. Thread 1.4 and Zigbee 3.0 are supported at chip level. Available protocol stacks, concurrent operating modes and application features depend on the selected firmware.

The module provides 60 peripheral pads and an EPAD ground connection designated as pin 61. The interface includes 54 GPIO-capable signals, a dedicated USB differential pair, power, enable/reset and ground. GPIO-capable signals include the six SD signals and the TX0/RX0 signals shown in Table 2.2.

GPIO routing supports interfaces such as UART, SPI, I2C, I2S, SD/MMC, CAN FD, Ethernet MAC, PWM and ADC, subject to the selected pins and firmware. Pin multiplexing does not permit all alternate functions to operate simultaneously. The dedicated USB pair is separate from GPIO multiplexing.

ESPS31-32 has 32 MB/16MB PSRAM and 4 MB, 8 MB or 16 MB external Flash options.

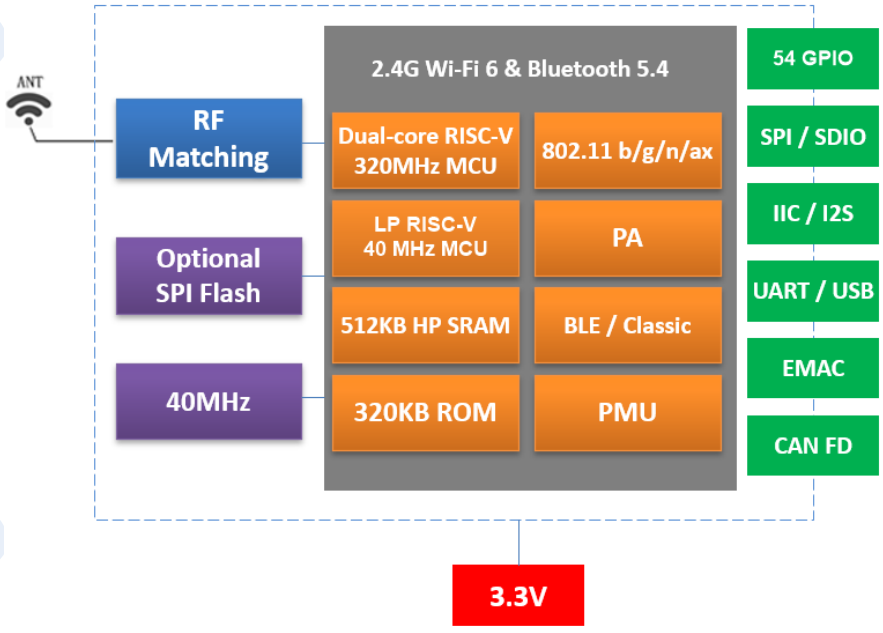


Fig.1.1 ESPS31-32 Module Structure

The main specifications of ESPS31-32 are summarized below.

Table 1.1 ESPS31-32 Specifications

Type	Item	Specification
Wi-Fi	Standard	IEEE 802.11 b/g/n/ax; 1T1R
	Channel frequency	2412–2484 MHz; regulatory-domain dependent
	Bandwidth	802.11 b/g/n: 20/40 MHz; 802.11ax: 20 MHz, non-AP mode
	Maximum PHY rate	150 Mbps (802.11n, HT40)
	Transmit / receive	Chip reference characteristics: see Section 6
	Antenna	PCB antenna
Bluetooth	Version	Bluetooth 5.4: LE and Classic Bluetooth
	LE PHY rate	125 kbps, 500 kbps, 1 Mbps and 2 Mbps
	Classic rate	Basic Rate: 1 Mbps; EDR: 2 Mbps and 3 Mbps
IEEE 802.15.4	Radio	2.4 GHz O-QPSK, 250 kbps
	Protocols	Thread 1.4; Zigbee 3.0; firmware dependent
Hardware	Chip	ESP32-S31NRV32/ESP32-S31NRV16
	HP processor	Dual-core RISC-V, up to 320 MHz
	LP processor	RISC-V, up to 40 MHz
	Internal memory	320 KB ROM; 512 KB HP SRAM; 32 KB LP SRAM
	PSRAM	16MB/32 MB, in package
	External Flash	4 MB / 8 MB / 16 MB; see module selection table
	Module pads	60 peripheral pads plus EPAD ground (pin 61)
	GPIO	54 GPIO-capable signals; includes SD and UART0 signals
	Interfaces	UART, SPI, I2C, I2S, SD/MMC, USB, CAN FD, Ethernet MAC, PWM and ADC; subject to pin multiplexing
	Supply	3.3 V nominal
	Dimensions	18 mm × 25.5 mm × 3 mm
Software	Wi-Fi modes	Station, SoftAP and promiscuous modes; Wi-Fi 6 is non-AP
	Security	WPA/WPA2/WPA3; supported modes depend on firmware
	Programming	UART0; USB download as supported by the boot configuration
	Development	ESP-IDF support is subject to the selected release and chip revision

2. Interface Definition

The module pinout is shown below. IO is the abbreviated form of GPIO. Pad numbers in this document refer to module pads.

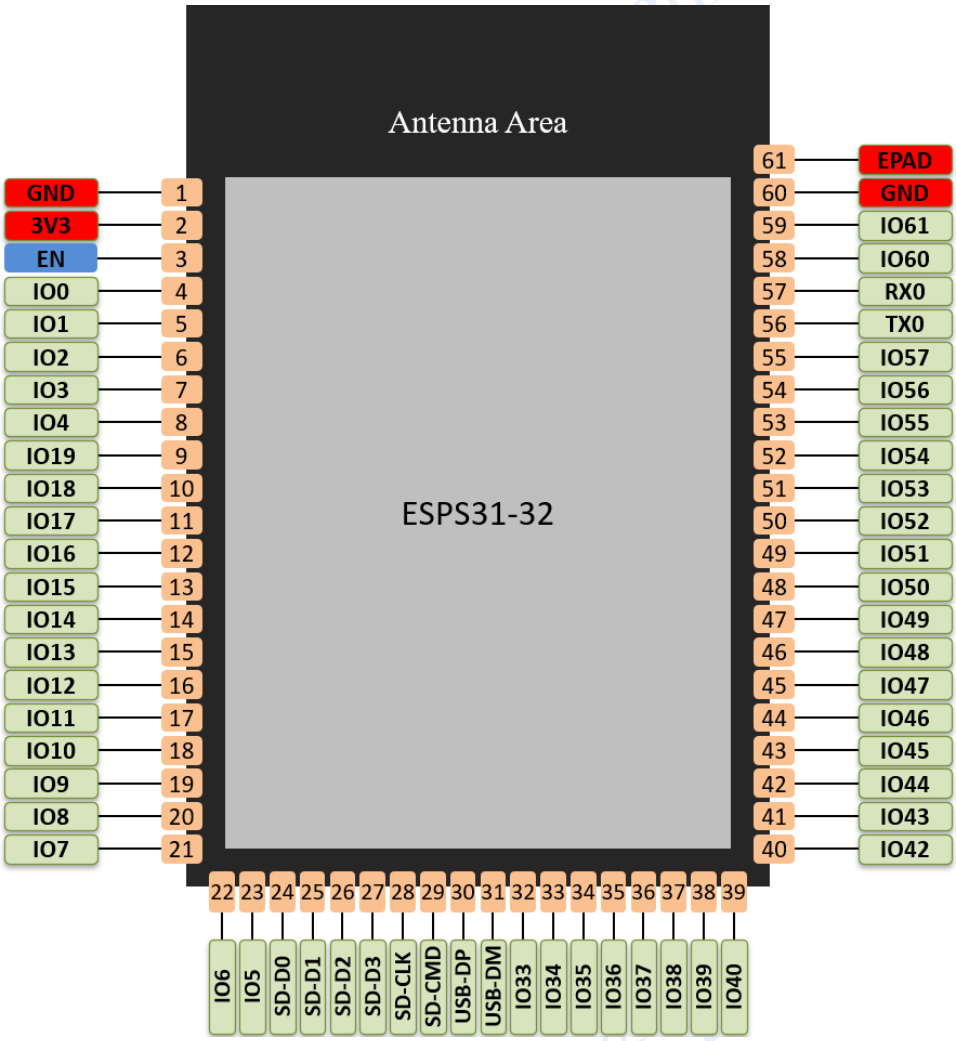


Fig. 2.1 ESPS31-32 Pin Definitions (Top View)

Boot strapping pins are sampled when reset is released. Use the boot settings below and avoid external circuitry that overrides the required levels during reset.

Table 2.1 Boot Mode

Mode	IO61
SPI boot mode (default)	1(HIGH)
Download boot mode	0 (LOW),Default

Table 2.2 Pin Functions (P: power; I: input; O: output; T: tri-state; A: analog)

No.	Pin Name	Type	Function

No.	Pin Name	Type	Function
1	GND	P	Ground
2	3V3	P	3.3 V power supply
3	EN	I	CHIP_PU; high: chip enabled; low: chip disabled; Default:10K pull-up
4	IO0	I/O	GPIO0; LP_GPIO0; LP_PROBE_TOP_OUT0; XTAL_32K_N
5	IO1	I/O	GPIO1; LP_GPIO1; LP_PROBE_TOP_OUT1; XTAL_32K_P
6	IO2	I/O	GPIO2; LCD_DATA19_OUT_PAD; LP_GPIO2; LP_UART_DTRN_PAD; LP_SPI_CK_PAD; LP_PROBE_TOP_OUT2
7	IO3	I/O	GPIO3; LCD_DATA20_OUT_PAD; LP_GPIO3; LP_UART_DSRN_PAD; LP_SPI_CS_PAD; LP_PROBE_TOP_OUT3
8	IO4	I/O	GPIO4; LCD_DATA21_OUT_PAD; LP_GPIO4; LP_UART_RTSN_PAD; LP_SPI_D_PAD; LP_PROBE_TOP_OUT4; DAC_CH0
9	IO19	I/O	GPIO19; SPI2_DQS_PAD; GMAC_PHY_RXD0_PAD; LCD_DATA11_OUT_PAD; TOUCH_CH13
10	IO18	I/O	GPIO18; SPI2_IO7_PAD; GMAC_PHY_RXD1_PAD; LCD_DATA10_OUT_PAD; TOUCH_CH12
11	IO17	I/O	GPIO17; SPI2_IO6_PAD; GMAC_PHY_RXD2_PAD; LCD_DATA9_OUT_PAD; TOUCH_CH11
12	IO16	I/O	GPIO16; SPI2_IO5_PAD; GMAC_PHY_RXD3_PAD; LCD_DATA8_OUT_PAD; TOUCH_CH10
13	IO15	I/O	GPIO15; SPI2_IO4_PAD; GMAC_PHY_RXDV_PAD; LCD_DATA7_OUT_PAD; TOUCH_CH9
14	IO14	I/O	GPIO14; SPI2_WP_PAD; GMAC_RX_CLK_PAD; LCD_DATA6_OUT_PAD; TOUCH_CH8
15	IO13	I/O	GPIO13; SPI2_Q_PAD; GMAC_RMII_CLK_PAD; LCD_DATA5_OUT_PAD; TOUCH_CH7
16	IO12	I/O	GPIO12; SPI2_CK_PAD; GMAC_PHY_TXEN_PAD; LCD_DATA4_OUT_PAD; TOUCH_CH6
17	IO11	I/O	GPIO11; SPI2_D_PAD; GMAC_PHY_TXD3_PAD; LCD_DATA3_OUT_PAD; TOUCH_CH5
18	IO10	I/O	GPIO10; SPI2_CS_PAD; GMAC_PHY_TXD2_PAD; LCD_DATA2_OUT_PAD; TOUCH_CH4
19	IO9	I/O	GPIO9; SPI2_HOLD_PAD; GMAC_PHY_TXD1_PAD; LCD_DATA1_OUT_PAD; TOUCH_CH3
20	IO8	I/O	GPIO8; GMAC_PHY_TXD0_PAD; LCD_DATA0_OUT_PAD; TOUCH_CH2
21	IO7	I/O	GPIO7; LCD_DATA23_OUT_PAD; LP_GPIO7; LP_UART_RXD_PAD; LP_I2C_SDA_PAD; LP_PROBE_TOP_OUT7; TOUCH_CH1
22	IO6	I/O	GPIO6; LP_GPIO6; LP_UART_TXD_PAD; LP_I2C_SCL_PAD; LP_PROBE_TOP_OUT6; TOUCH_CH0
23	IO5	I/O	GPIO5; LCD_DATA22_OUT_PAD; LP_GPIO5; LP_UART_CTSN_PAD; LP_SPI_Q_PAD; LP_PROBE_TOP_OUT5; DAC_CH1
24	SD-D0	I/O	GPIO20; SDIO_DATA0; SPI2_CK_PAD
25	SD-D1	I/O	GPIO21; SDIO_DATA1; SPI2_D_PAD
26	SD-D2	I/O	GPIO22; SDIO_DATA2; SPI2_Q_PAD

No.	Pin Name	Type	Function
27	SD-D3	I/O	GPIO23; SDIO_DATA3; SPI2_CS_PAD
28	SD-CLK	I/O	GPIO24; SDIO_CLK; SPI2_HOLD_PAD
29	SD-CMD	I/O	GPIO25; SDIO_CMD; SPI2_WP_PAD
30	USB-DP	I/O	USB_DP; USB 2.0 High-Speed OTG PHY D+
31	USB-DM	I/O	USB_DM; USB 2.0 High-Speed OTG PHY D-
32	IO33	I/O	GPIO33; LCD_DATA12_OUT_PAD; USB1P1_N0
33	IO34	I/O	GPIO34; LCD_DATA13_OUT_PAD; USB1P1_P0
34	IO35	I/O	GPIO35; REF_GMAC_CLK_PAD; LCD_DATA14_OUT_PAD; SD2_CDATA0_PAD
35	IO36	I/O	GPIO36; LCD_DATA15_OUT_PAD; SD2_CDATA1_PAD
36	IO37	I/O	GPIO37; LCD_DATA16_OUT_PAD; SD2_CDATA2_PAD; PAD_COMP0
37	IO38	I/O	GPIO38; LCD_DATA17_OUT_PAD; SD2_CDATA3_PAD; PAD_COMP1
38	IO39	I/O	GPIO39; LCD_DATA18_OUT_PAD; SD2_CCLK_PAD; PAD_COMP2
39	IO40	I/O	GPIO40; LCD_PCLK_PAD; SD2_CCMD_PAD; PAD_COMP3
40	IO42	I/O	GPIO42; ADC1_CH0_N
41	IO43	I/O	GPIO43; LCD_H_ENABLE_PAD; ADC1_CH0_P
42	IO44	I/O	GPIO44; LCD_H_SYNC_PAD; ADC1_CH1_N
43	IO45	I/O	GPIO45; LCD_V_SYNC_PAD; ADC1_CH1_P
44	IO46	I/O	GPIO46; CAM_DATA0_IN_PAD; ADC1_CH2_N
45	IO47	I/O	GPIO47; CAM_DATA1_IN_PAD; ADC1_CH2_P
46	IO48	I/O	GPIO48; CAM_DATA2_IN_PAD; ADC1_CH3_N
47	IO49	I/O	GPIO49; CAM_DATA3_IN_PAD; ADC1_CH3_P
48	IO50	I/O	GPIO50; CAM_DATA4_IN_PAD; ADC2_CH0_N
49	IO51	I/O	GPIO51; CAM_DATA5_IN_PAD; ADC2_CH0_P
50	IO52	I/O	GPIO52; SPI2_CS_PAD; CAM_DATA6_IN_PAD; ADC2_CH1_N
51	IO53	I/O	GPIO53; SPI2_CK_PAD; CAM_DATA7_IN_PAD; ADC2_CH1_P
52	IO54	I/O	GPIO54; MTDO; SPI2_D_PAD; CAM_PCLK_PAD; ADC2_CH2_N
53	IO55	I/O	GPIO55; MTCK; SPI2_Q_PAD; CAM_XCLK_PAD; ADC2_CH2_P
54	IO56	I/O	GPIO56; MTDI; SPI2_HOLD_PAD; CAM_V_SYNC_PAD; ADC2_CH3_N

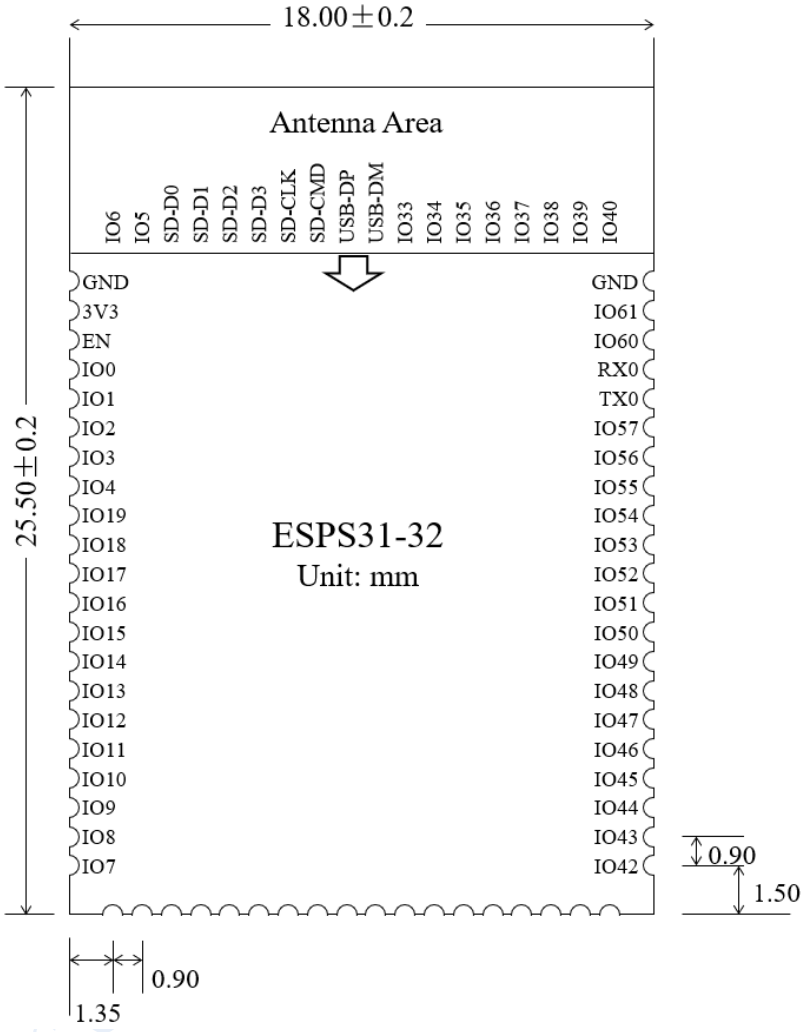
No.	Pin Name	Type	Function
55	IO57	I/O	GPIO57; MTMS; SPI2_WP_PAD; CAM_H_SYNC_PAD; ADC2_CH3_P
56	TX0	I/O	GPIO58; UART0_TXD_PAD
57	RX0	I/O	GPIO59; UART0_RXD_PAD
58	IO60	I/O	GPIO60
59	IO61	I/O	GPIO61
60	GND	P	Ground
61	EPAD	P	Exposed pad; connect to GND

3. Size and Layout

The outline and PCB footprint drawings below define the module dimensions and pad arrangement. Dimensions are in millimetres.



Fig. 3.1 Shape for ESPS31-32



(a) Top View

(b) Side View

Fig. 3.2 ESPS31-32 Dimensions

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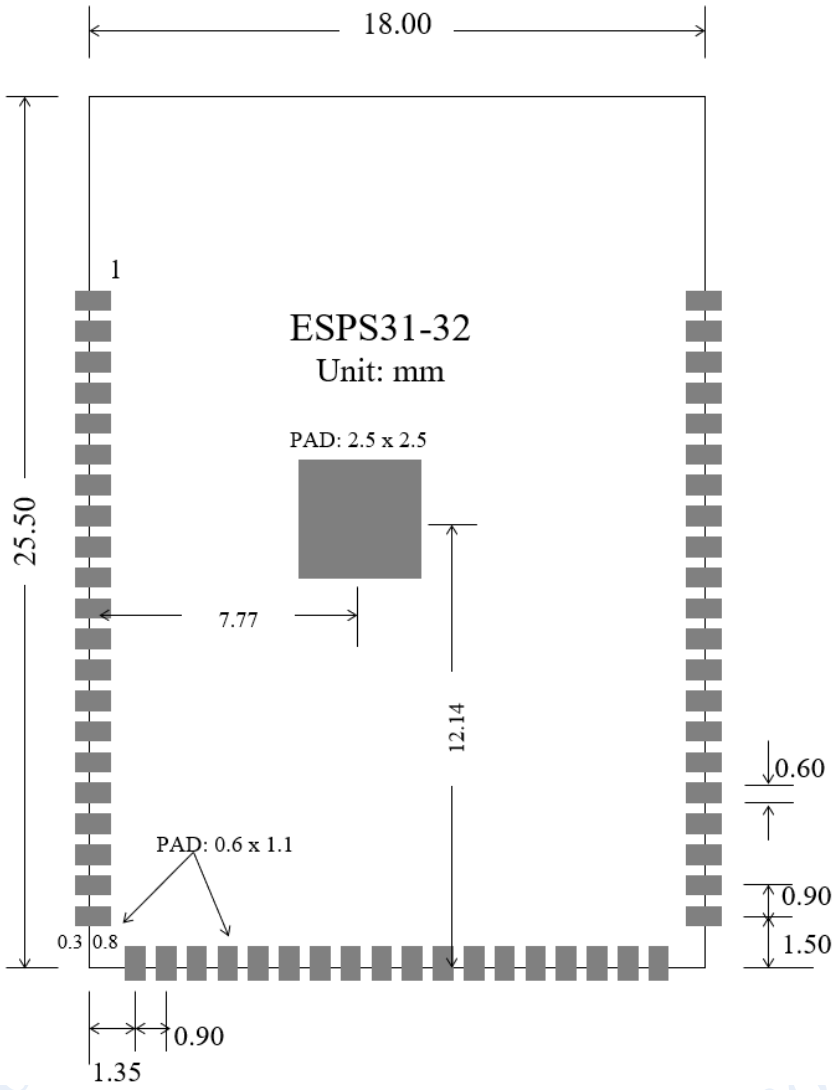

Fig. 3.3 ESPS31-32 PCB Footprint

4. Electrical Characteristics

Table 4.1 Electrical Characteristics

Parameter	Condition	Min	Typical	Max	Unit
VDDA input voltage	VDDA1, VDDA2, VDDA3, VDDA4	3.0	3.3	3.6	V
VDDPST input voltage	VDDPST_1, VDDPST_2, VDDPST_3, VDDPST_4	3.0	3.3	3.6	V
Supply current capability	IVDD; recommended cumulative input-current capability	0.6	-	-	A
Operating ambient temperature	ESP32-S31NRV32 chip reference	-40	-	85	°C
VIH	High-level input voltage; VDD = respective pad supply	0.75 × VDD	-	VDD + 0.3	V
VIL	Low-level input voltage; VDD = respective pad supply	-0.3	-	0.25 × VDD	V

Parameter	Condition	Min	Typical	Max	Unit
VOH	High-level output voltage; high-impedance load	0.8 × VDD	-	-	V
VOL	Low-level output voltage; high-impedance load	-	-	0.1 × VDD	V
tSTBL	Power rails stable before CHIP_PU rises	1	-	-	ms
tRST	CHIP_PU held below VIL_nRST to reset the chip	1	-	-	ms

5. Power Consumption

Table 5.1 ESP32-S31 Chip Reference Power Consumption

Parameter	Min	Typical	Peak	Unit
Wi-Fi TX: 802.11b, 1 Mbps, DSSS, 21 dBm	-	-	377	mA
Wi-Fi TX: 802.11g, 54 Mbps, OFDM, 18 dBm	-	-	297	mA
Wi-Fi TX: 802.11n, HT20, MCS7, 18 dBm	-	-	299	mA
Wi-Fi TX: 802.11n, HT40, MCS7, 17 dBm	-	-	300	mA
Wi-Fi TX: 802.11ax, MCS9, 15 dBm	-	-	265	mA
Wi-Fi RX: 802.11b/g/n, HT20	-	-	110	mA
Wi-Fi RX: 802.11n, HT40	-	-	117	mA
Wi-Fi RX: 802.11ax, HE20	-	-	112	mA
Bluetooth LE TX: 20 dBm	-	-	340	mA
Bluetooth LE TX: 11 dBm	-	-	225	mA
Bluetooth LE TX: 0 dBm	-	-	160	mA
Bluetooth LE TX: -17.5 dBm	-	-	120	mA
Bluetooth LE RX	-	-	105	mA
Bluetooth Classic TX: 12 dBm	-	-	225	mA
Bluetooth Classic TX: 6 dBm	-	-	185	mA
Bluetooth Classic TX: 0 dBm	-	-	145	mA
Bluetooth Classic TX: -17.5 dBm	-	-	116	mA
Bluetooth Classic RX	-	-	96	mA
IEEE 802.15.4 TX: 19 dBm	-	-	310	mA
IEEE 802.15.4 TX: 13 dBm	-	-	230	mA

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Parameter	Min	Typical	Peak	Unit
IEEE 802.15.4 TX: 1 dBm	-	-	170	mA
IEEE 802.15.4 TX: -17.5 dBm	-	-	120	mA
IEEE 802.15.4 RX	-	-	104	mA
Modem-sleep, 320 MHz: dual-core WAITI; peripheral clocks disabled	-	25	-	mA
Modem-sleep, 320 MHz: dual-core WAITI; peripheral clocks enabled	-	75	-	mA
Modem-sleep, 320 MHz: dual-core CoreMark; peripheral clocks disabled	-	91	-	mA
Modem-sleep, 320 MHz: dual-core CoreMark; peripheral clocks enabled	-	147	-	mA
Modem-sleep, 320 MHz: core 0 WAITI, core 1 SIMD; peripheral clocks disabled	-	64	-	mA
Modem-sleep, 320 MHz: core 0 WAITI, core 1 SIMD; peripheral clocks enabled	-	114	-	mA
Modem-sleep, 320 MHz: core 0 CoreMark, core 1 SIMD; peripheral clocks disabled	-	100	-	mA
Modem-sleep, 320 MHz: core 0 CoreMark, core 1 SIMD; peripheral clocks enabled	-	152	-	mA
Light-sleep: GPIOs high-impedance; all power supplies enabled	-	1	-	mA
Light-sleep: GPIOs high-impedance; most peripherals disabled; USB connected	-	0.07	-	mA
Light-sleep: all peripherals disabled; HP memory data retained	-	0.05	-	mA
Deep-sleep: LP timer and LP memory powered on	-	0.012	-	mA
Power off: CHIP_PU low	-	0.001	-	mA

The peak current consumption of ESPS31-32 exceeds 500mA when the module starts work (RF calibration work consumes maximum current). Therefore, the recommended power supply is no less than 500mA.

Power modes:

1. Active: processors, peripherals and radios operate as enabled by firmware.

2. Modem-sleep: radio circuits can be powered down while the application processor remains active; current depends on CPU and peripheral configuration.

3. Light-sleep: selected state is retained while clocks and power domains are managed for reduced consumption. Wake-up sources and connectivity retention depend on the configuration.

4. Deep-sleep: high-performance resources are powered down; selected low-power resources remain available for retention and wake-up.

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6. Wi-Fi RF Characteristics

The following tables contain ESPS31-32 module RF characteristics. RF reference test conditions: 3.3 V ±5% supply and 25°C ambient unless otherwise specified.

Table 6.1 Wi-Fi Transmit Characteristics

Parameter	Min	Typical	Max	Unit
802.11b, 1 Mbps, DSSS	-	20.0	-	dBm
802.11b, 11 Mbps, CCK	-	19.5	-	dBm
802.11g, 6 Mbps, OFDM	-	19.5	-	dBm
802.11g, 54 Mbps, OFDM	-	17.8	-	dBm
802.11n, HT20, MCS0	-	18.0	-	dBm
802.11n, HT20, MCS7	-	17.2	-	dBm
802.11n, HT40, MCS0	-	18.8	-	dBm
802.11n, HT40, MCS7	-	15.9	-	dBm
802.11ax, HE20, MCS0	-	18.5	-	dBm
802.11ax, HE20, MCS9	-	14.5	-	dBm
EVM, 802.11b, 1 Mbps, DSSS at 21.0 dBm TX power	-	-25.0	-10.0	dB
EVM, 802.11b, 11 Mbps, CCK at 21.0 dBm TX power	-	-25.0	-10.0	dB
EVM, 802.11g, 6 Mbps, OFDM at 20.0 dBm TX power	-	-24.0	-5.0	dB
EVM, 802.11g, 54 Mbps, OFDM at 18.0 dBm TX power	-	-30.0	-25.0	dB
EVM, 802.11n, HT20, MCS0 at 20.0 dBm TX power	-	-22.0	-5.0	dB
EVM, 802.11n, HT20, MCS7 at 18.0 dBm TX power	-	-30.0	-27.0	dB
EVM, 802.11n, HT40, MCS0 at 19.0 dBm TX power	-	-26.0	-5.0	dB
EVM, 802.11n, HT40, MCS7 at 17.0 dBm TX power	-	-31.0	-27.0	dB
EVM, 802.11ax, HE20, MCS0 at 20.0 dBm TX power	-	-23.0	-5.0	dB
EVM, 802.11ax, HE20, MCS9 at 15.0 dBm TX power	-	-34.0	-32.0	dB

Table 6.2 Wi-Fi Receive Characteristics

Parameter	Min	Typical	Max	Unit
Sensitivity, 802.11b, 1 Mbps, DSSS	-	-97.5	-	dBm

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Parameter	Min	Typical	Max	Unit
Sensitivity, 802.11b, 2 Mbps, DSSS	-	-95.5	-	dBm
Sensitivity, 802.11b, 5.5 Mbps, CCK	-	-92.2	-	dBm
Sensitivity, 802.11b, 11 Mbps, CCK	-	-88.5	-	dBm
Sensitivity, 802.11g, 6 Mbps, OFDM	-	-93.0	-	dBm
Sensitivity, 802.11g, 9 Mbps, OFDM	-	-91.5	-	dBm
Sensitivity, 802.11g, 12 Mbps, OFDM	-	-91.5	-	dBm
Sensitivity, 802.11g, 18 Mbps, OFDM	-	-87.5	-	dBm
Sensitivity, 802.11g, 24 Mbps, OFDM	-	-86.5	-	dBm
Sensitivity, 802.11g, 36 Mbps, OFDM	-	-82.0	-	dBm
Sensitivity, 802.11g, 48 Mbps, OFDM	-	-77.0	-	dBm
Sensitivity, 802.11g, 54 Mbps, OFDM	-	-75.5	-	dBm
Sensitivity, 802.11n, HT20, MCS0	-	-92.5	-	dBm
Sensitivity, 802.11n, HT20, MCS1	-	-91.0	-	dBm
Sensitivity, 802.11n, HT20, MCS2	-	-83.5	-	dBm
Sensitivity, 802.11n, HT20, MCS3	-	-84.0	-	dBm
Sensitivity, 802.11n, HT20, MCS4	-	-81.5	-	dBm
Sensitivity, 802.11n, HT20, MCS5	-	-75.5	-	dBm
Sensitivity, 802.11n, HT20, MCS6	-	-76.0	-	dBm
Sensitivity, 802.11n, HT20, MCS7	-	-75.0	-	dBm
Sensitivity, 802.11n, HT40, MCS0	-	-90.0	-	dBm
Sensitivity, 802.11n, HT40, MCS1	-	-89.5	-	dBm
Sensitivity, 802.11n, HT40, MCS2	-	-85.0	-	dBm
Sensitivity, 802.11n, HT40, MCS3	-	-82.5	-	dBm
Sensitivity, 802.11n, HT40, MCS4	-	-80.5	-	dBm
Sensitivity, 802.11n, HT40, MCS5	-	-76.0	-	dBm
Sensitivity, 802.11n, HT40, MCS6	-	-74.5	-	dBm
Sensitivity, 802.11n, HT40, MCS7	-	-73.5	-	dBm
Sensitivity, 802.11ax, HE20, MCS0	-	-91.0	-	dBm

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Parameter	Min	Typical	Max	Unit
Sensitivity, 802.11ax, HE20, MCS1	-	-90.0	-	dBm
Sensitivity, 802.11ax, HE20, MCS2	-	-88.0	-	dBm
Sensitivity, 802.11ax, HE20, MCS3	-	-85.5	-	dBm
Sensitivity, 802.11ax, HE20, MCS4	-	-82.0	-	dBm
Sensitivity, 802.11ax, HE20, MCS5	-	-78.0	-	dBm
Sensitivity, 802.11ax, HE20, MCS6	-	-72.5	-	dBm
Sensitivity, 802.11ax, HE20, MCS7	-	-73.5	-	dBm
Sensitivity, 802.11ax, HE20, MCS8	-	-70.0	-	dBm
Sensitivity, 802.11ax, HE20, MCS9	-	-65.5	-	dBm
Maximum RX level, 802.11b, 1 Mbps, DSSS	-	5	-	dBm
Maximum RX level, 802.11b, 11 Mbps, CCK	-	5	-	dBm
Maximum RX level, 802.11g, 6 Mbps, OFDM	-	5	-	dBm
Maximum RX level, 802.11g, 54 Mbps, OFDM	-	0	-	dBm
Maximum RX level, 802.11n, HT20, MCS0	-	5	-	dBm
Maximum RX level, 802.11n, HT20, MCS7	-	0	-	dBm
Maximum RX level, 802.11n, HT40, MCS0	-	5	-	dBm
Maximum RX level, 802.11n, HT40, MCS7	-	0	-	dBm
Maximum RX level, 802.11ax, HE20, MCS0	-	5	-	dBm
Maximum RX level, 802.11ax, HE20, MCS9	-	0	-	dBm

Table 6.3 Wi-Fi Adjacent Channel Rejection

Parameter	Min	Typical	Max	Unit
802.11b, 1 Mbps, DSSS	-	43	-	dB
802.11b, 11 Mbps, CCK	-	40	-	dB
802.11g, 6 Mbps, OFDM	-	33	-	dB
802.11g, 54 Mbps, OFDM	-	18	-	dB
802.11n, HT20, MCS0	-	30	-	dB
802.11n, HT20, MCS7	-	15	-	dB
802.11n, HT40, MCS0	-	23	-	dB

Parameter	Min	Typical	Max	Unit
802.11n, HT40, MCS7	-	10	-	dB
802.11ax, HE20, MCS0	-	25	-	dB
802.11ax, HE20, MCS9	-	2	-	dB

7. Bluetooth LE Radio

Table 7.1 Bluetooth LE Transmit Characteristics

Parameter	Min	Typical	Max	Unit
RF transmit power range	-17.5	-	20	dBm
1 Mbps: Carrier offset/drift, max |f_n|, n=0,1,2,3,...k	-	0.5	-	kHz
1 Mbps: Carrier offset/drift, max |f_0 - f_n|, n=2,3,4,...k	-	1.0	-	kHz
1 Mbps: Carrier offset/drift, max |f_n - f_(n-5)|, n=6,7,8,...k	-	1.0	-	kHz
1 Mbps: Carrier offset/drift, f_1 - f_0	-	1.4	-	kHz
1 Mbps: Modulation, Delta F1avg	-	256.3	-	kHz
1 Mbps: Modulation, min Delta F2max for at least 99.9% of all Delta F2max	-	252.6	-	kHz
1 Mbps: Modulation, Delta F2avg / Delta F1avg	-	0.95	-	-
1 Mbps: In-band emissions, +/-2 MHz offset	-	-29	-	dBm
1 Mbps: In-band emissions, +/-3 MHz offset	-	-38	-	dBm
1 Mbps: In-band emissions, greater than +/-3 MHz offset	-	-44	-	dBm
2 Mbps: Carrier offset/drift, max |f_n|, n=0,1,2,3,...k	-	0.5	-	kHz
2 Mbps: Carrier offset/drift, max |f_0 - f_n|, n=2,3,4,...k	-	1.3	-	kHz
2 Mbps: Carrier offset/drift, max |f_n - f_(n-5)|, n=6,7,8,...k	-	0.9	-	kHz
2 Mbps: Carrier offset/drift, f_1 - f_0	-	0.5	-	kHz
2 Mbps: Modulation, Delta F1avg	-	508.2	-	kHz
2 Mbps: Modulation, min Delta F2max for at least 99.9% of all Delta F2max	-	516.9	-	kHz
2 Mbps: Modulation, Delta F2avg / Delta F1avg	-	0.97	-	-
2 Mbps: In-band emissions, +/-4 MHz offset	-	-43	-	dBm
2 Mbps: In-band emissions, +/-5 MHz offset	-	-45	-	dBm
2 Mbps: In-band emissions, greater than +/-5 MHz offset	-	-48	-	dBm

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Parameter	Min	Typical	Max	Unit
125 Kbps: Carrier offset/drift, max |f_n|, n=0,1,2,3,...k	-	1.3	-	kHz
125 Kbps: Carrier offset/drift, max |f_0 - f_n|, n=1,2,3,...k	-	0.5	-	kHz
125 Kbps: Carrier offset/drift, f_0 - f_3	-	0.1	-	kHz
125 Kbps: Carrier offset/drift, max |f_n - f_(n-3)|, n=7,8,9,...k	-	0.6	-	kHz
125 Kbps: Modulation, Delta F1avg	-	255.7	-	kHz
125 Kbps: Modulation, min Delta F1max for at least 99.9% of all Delta F1max	-	261.9	-	kHz
125 Kbps: In-band emissions, +/-2 MHz offset	-	-26	-	dBm
125 Kbps: In-band emissions, +/-3 MHz offset	-	-36	-	dBm
125 Kbps: In-band emissions, greater than +/-3 MHz offset	-	-40	-	dBm
500 Kbps: Carrier offset/drift, max |f_n|, n=0,1,2,3,...k	-	0.7	-	kHz
500 Kbps: Carrier offset/drift, max |f_0 - f_n|, n=1,2,3,...k	-	0.5	-	kHz
500 Kbps: Carrier offset/drift, f_0 - f_3	-	0.1	-	kHz
500 Kbps: Carrier offset/drift, max |f_n - f_(n-3)|, n=7,8,9,...k	-	0.6	-	kHz
500 Kbps: Modulation, Delta F2avg	-	245.7	-	kHz
500 Kbps: Modulation, min Delta F2max for at least 99.9% of all Delta F2max	-	252.9	-	kHz
500 Kbps: In-band emissions, +/-2 MHz offset	-	-30	-	dBm
500 Kbps: In-band emissions, +/-3 MHz offset	-	-40	-	dBm
500 Kbps: In-band emissions, greater than +/-3 MHz offset	-	-45	-	dBm

Table 7.2 Bluetooth LE Receive Characteristics

Parameter	Min	Typical	Max	Unit
1 Mbps: Sensitivity at 30.8% PER	-	-98.0	-	dBm
1 Mbps: Maximum received signal at 30.8% PER	-	8	-	dBm
1 Mbps: C/I, co-channel, F = F0	-	7	-	dB
1 Mbps: C/I, adjacent channel, F = F0 + 1 MHz	-	-2	-	dB
1 Mbps: C/I, adjacent channel, F = F0 - 1 MHz	-	-4	-	dB
1 Mbps: C/I, adjacent channel, F = F0 + 2 MHz	-	-29	-	dB
1 Mbps: C/I, adjacent channel, F = F0 - 2 MHz	-	-32	-	dB

Parameter	Min	Typical	Max	Unit
1 Mbps: C/I, adjacent channel, F = F0 + 3 MHz	-	-30	-	dB
1 Mbps: C/I, adjacent channel, F = F0 - 3 MHz	-	-43	-	dB
1 Mbps: C/I, adjacent channel, F >= F0 + 4 MHz	-	-31	-	dB
1 Mbps: C/I, adjacent channel, F <= F0 - 4 MHz	-	-46	-	dB
1 Mbps: C/I, image frequency	-	-20	-	dB
1 Mbps: C/I, F = Fimage + 1 MHz	-	-31	-	dB
1 Mbps: C/I, F = Fimage - 1 MHz	-	-30	-	dB
1 Mbps: Out-of-band blocking, 30-2000 MHz	-	-25	-	dBm
1 Mbps: Out-of-band blocking, 2003-2399 MHz	-	-30	-	dBm
1 Mbps: Out-of-band blocking, 2484-2997 MHz	-	-30	-	dBm
1 Mbps: Out-of-band blocking, 3000 MHz-12.75 GHz	-	-25	-	dBm
1 Mbps: Intermodulation	-	-43	-	dBm
2 Mbps: Sensitivity at 30.8% PER	-	-94.5	-	dBm
2 Mbps: Maximum received signal at 30.8% PER	-	8	-	dBm
2 Mbps: C/I, co-channel, F = F0	-	9	-	dB
2 Mbps: C/I, adjacent channel, F = F0 + 2 MHz	-	-6	-	dB
2 Mbps: C/I, adjacent channel, F = F0 - 2 MHz	-	-8	-	dB
2 Mbps: C/I, adjacent channel, F = F0 + 4 MHz	-	-18	-	dB
2 Mbps: C/I, adjacent channel, F = F0 - 4 MHz	-	-36	-	dB
2 Mbps: C/I, adjacent channel, F = F0 + 6 MHz	-	-37	-	dB
2 Mbps: C/I, adjacent channel, F = F0 - 6 MHz	-	-42	-	dB
2 Mbps: C/I, adjacent channel, F >= F0 + 8 MHz	-	-45	-	dB
2 Mbps: C/I, adjacent channel, F <= F0 - 8 MHz	-	-44	-	dB
2 Mbps: C/I, image frequency	-	-18	-	dB
2 Mbps: C/I, F = Fimage + 2 MHz	-	-37	-	dB
2 Mbps: C/I, F = Fimage - 2 MHz	-	-6	-	dB
2 Mbps: Out-of-band blocking, 30-2000 MHz	-	-25	-	dBm
2 Mbps: Out-of-band blocking, 2003-2399 MHz	-	-30	-	dBm

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Parameter	Min	Typical	Max	Unit
2 Mbps: Out-of-band blocking, 2484-2997 MHz	-	-30	-	dBm
2 Mbps: Out-of-band blocking, 3000 MHz-12.75 GHz	-	-25	-	dBm
2 Mbps: Intermodulation	-	-31	-	dBm
125 Kbps: Sensitivity at 30.8% PER	-	-105.0	-	dBm
125 Kbps: Maximum received signal at 30.8% PER	-	8	-	dBm
125 Kbps: C/I, co-channel, F = F0	-	2	-	dB
125 Kbps: C/I, adjacent channel, F = F0 + 1 MHz	-	-6	-	dB
125 Kbps: C/I, adjacent channel, F = F0 - 1 MHz	-	-3	-	dB
125 Kbps: C/I, adjacent channel, F = F0 + 2 MHz	-	-26	-	dB
125 Kbps: C/I, adjacent channel, F = F0 - 2 MHz	-	-37	-	dB
125 Kbps: C/I, adjacent channel, F = F0 + 3 MHz	-	-33	-	dB
125 Kbps: C/I, adjacent channel, F = F0 - 3 MHz	-	-51	-	dB
125 Kbps: C/I, adjacent channel, F >= F0 + 4 MHz	-	-33	-	dB
125 Kbps: C/I, adjacent channel, F <= F0 - 4 MHz	-	-54	-	dB
125 Kbps: C/I, image frequency	-	-28	-	dB
125 Kbps: C/I, F = Fimage + 1 MHz	-	-33	-	dB
125 Kbps: C/I, F = Fimage - 1 MHz	-	-33	-	dB
500 Kbps: Sensitivity at 30.8% PER	-	-101.0	-	dBm
500 Kbps: Maximum received signal at 30.8% PER	-	8	-	dBm
500 Kbps: C/I, co-channel, F = F0	-	4	-	dB
500 Kbps: C/I, adjacent channel, F = F0 + 1 MHz	-	-5	-	dB
500 Kbps: C/I, adjacent channel, F = F0 - 1 MHz	-	-4	-	dB
500 Kbps: C/I, adjacent channel, F = F0 + 2 MHz	-	-31	-	dB
500 Kbps: C/I, adjacent channel, F = F0 - 2 MHz	-	-42	-	dB
500 Kbps: C/I, adjacent channel, F = F0 + 3 MHz	-	-34	-	dB
500 Kbps: C/I, adjacent channel, F = F0 - 3 MHz	-	-55	-	dB
500 Kbps: C/I, adjacent channel, F >= F0 + 4 MHz	-	-32	-	dB
500 Kbps: C/I, adjacent channel, F <= F0 - 4 MHz	-	-58	-	dB

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Parameter	Min	Typical	Max	Unit
500 Kbps: C/I, image frequency	-	-24	-	dB
500 Kbps: C/I, F = Fimage + 1 MHz	-	-32	-	dB
500 Kbps: C/I, F = Fimage - 1 MHz	-	-34	-	dB

8. IEEE 802.15.4 Radio

Table 8.1 IEEE 802.15.4 Transmit Characteristics

Parameter	Min	Typical	Max	Unit
RF transmit power range	-17.5	-	19.0	dBm
EVM	-	24.0%	-	-

Table 8.2 IEEE 802.15.4 Receive Characteristics

Parameter	Min	Typical	Max	Unit
Sensitivity at 1% PER	-	-102.0	-	dBm
Maximum received signal at 1% PER	-	8	-	dBm
Relative jamming level, adjacent channel, F = F0 + 5 MHz	-	-30	-	dB
Relative jamming level, adjacent channel, F = F0 - 5 MHz	-	-40	-	dB
Relative jamming level, alternate channel, F = F0 + 10 MHz	-	-52	-	dB
Relative jamming level, alternate channel, F = F0 - 10 MHz	-	-53	-	dB

9. Recommended Reflow Soldering Profile

(1) Maximum number of reflow cycles: 2

(2) Maximum heating rate: 3° C/s

(3) Maximum cooling rate: 3° C/s

(4) Time above 217° C: 60–120 s

(5) Peak temperature: 240 – 250° C. Confirm the assembly profile against the solder paste and component requirements.

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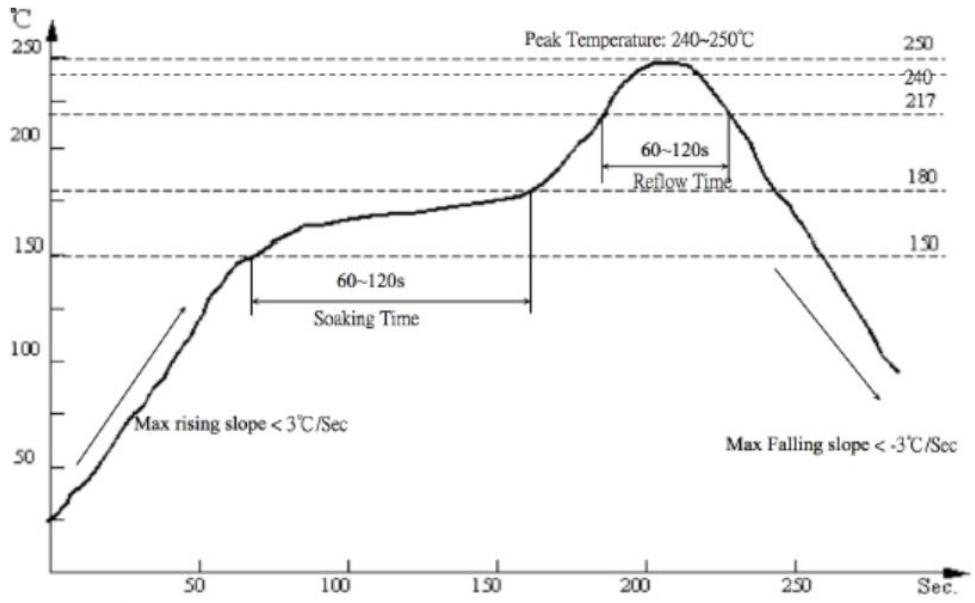

Fig. 9.1 Recommended Reflow Profile

10. Minimum System Design

Connect a regulated 3.3 V supply, a continuous ground return, reset/enable control and the selected programming interface.

Design notes:

(1) Connect pin 2 (3V3), pins 1 and 60 (GND), and the EPAD ground connection. Place supply decoupling close to the module and keep the power and ground paths short.

(2) EN (pin 3) is the active-high chip-enable input; drive it low to reset the chip.

(3) Set the required boot strapping levels before releasing EN. The boot-mode settings are listed in Table 2.1.

(4) UART0 uses TX0 (pin 56) and RX0 (pin 57). Connect module TX0 to host RX and module RX0 to host TX, with a common ground and compatible logic levels. Pins 30 and 31 are the dedicated USB D+ and D− signals.

11. Recommended Layout Design

For the best RF performance, place the PCB antenna at the edge of the host board. Keep the antenna region clear of copper, traces, components, metal enclosures and cables. The examples below illustrate placement principles; validate RF performance in the final enclosure.

Preferred placement: extend the antenna region beyond the edge of the host PCB, with free space around and beneath the antenna.

Alternative placement: provide a host-board cutout beneath the antenna and preserve the clearances shown in the drawing.

If the antenna lies above the host PCB, keep the area beneath and around it free of copper, routing and components on every layer. This placement should be verified by RF testing.

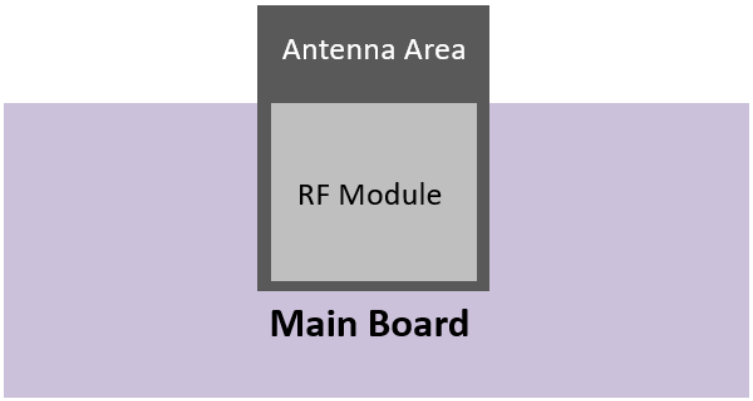

Fig.11.1 Solution 1

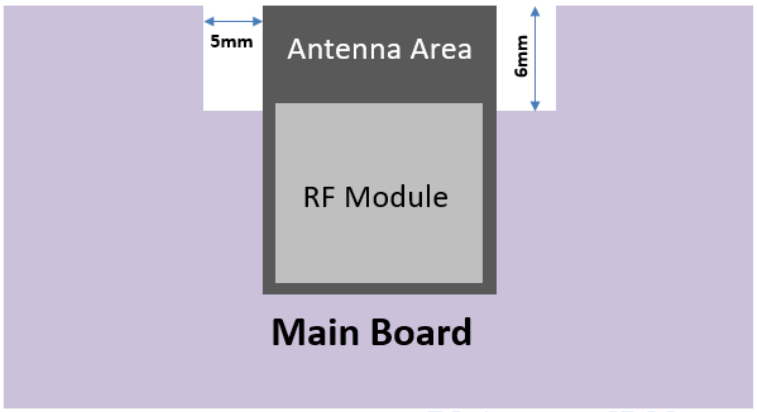

Fig.11.2 Solution 2

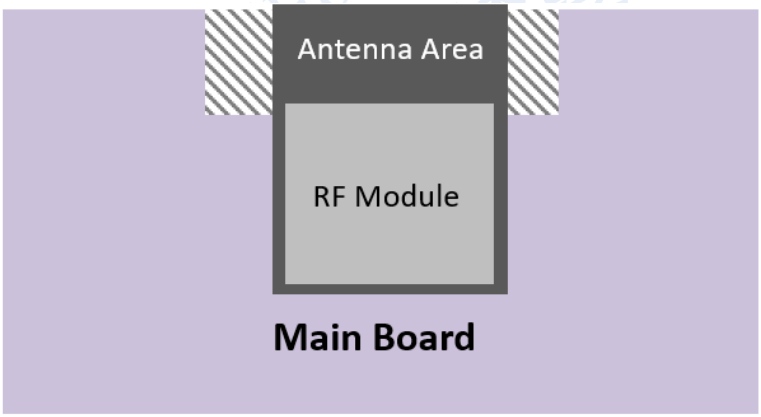

Fig.11.3 Solution 3

12. Peripheral Design Recommendations

Route USB differential signals with controlled impedance, matched routing and a continuous ground reference. Select termination and damping components for the specific interface and board layout; do not apply a generic series-resistor value to every signal. Provide suitable ESD protection at externally accessible connectors. Series resistance alone does not establish ESD protection.

13. Product Handling

13.1 Storage Conditions

Keep modules in their supplied moisture-barrier packaging until assembly. Follow the package label for moisture sensitivity, floor life, storage and baking requirements. Avoid condensation and protect the antenna, shield and pads from mechanical damage.

13.2 Electrostatic Discharge (ESD)

Handle modules in an ESD-controlled work area with grounded personnel and suitable equipment.

Chip-level ESD ratings do not establish the ESD immunity of the complete module or end product. Protect external interfaces as required by the application.

14. Packaging Instructions

The packaging illustration below shows reel packaging inside a moisture-barrier bag. Confirm the delivery format and quantity against the order and package label.

Each inner box contains 550 modules and measures 340 × 360 × 60 mm. An outer carton contains five inner boxes (2,750 modules) and measures 355 × 375 × 325 mm. Packaging configuration is subject to the confirmed order.

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Fig. 14.1 Module Packaging

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Appendix: Design References

